Refine Search

Search Results -

Terms	Documents
L1.clm. and (configur$5 same multiplex$3).clm.	6

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, June 22, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB; PLUR=YES; OP=OR			
L3	l1.clm. and (configur$5 same multiplex$3).clm.	6	L3
L2	l1 and (configur$5 same multiplex$3)	44	L2
L1	"first bus" same "second bus" same multiplex$3	96	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
"first bus" same "second bus" same multiplex$3	351

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, June 22, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	"first bus" same "second bus" same multiplex$3	351	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
"first bus" same "second bus" same multiplex$3	46

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

L2

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Thursday, June 22, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	"first bus" same "second bus" same multiplex$3	46	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	"first bus" same "second bus" same multiplex$3	351	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/253 |713/1 |713/323 |716/12 |370/464 |370/362 |370/364 |370/357 |370/916 |712/29 |710/316 |710/302 |710/303 |710/304 |710/104 |710/72 |710/305 |710/107 |710/307 |710/317 |710/37).ccls.	10927

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, June 22, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L3	710/316,302-304,104,72,305,107,307,317,37;713/1,323;370/464,362,364,357,916;712/29;709/253;716/12.ccls.	10927	L3
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L2	"first bus" same "second bus" same multiplex$3	46	L2
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L1	"first bus" same "second bus" same multiplex$3	351	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L4 and (configur$5 same multiplex$3)	23

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

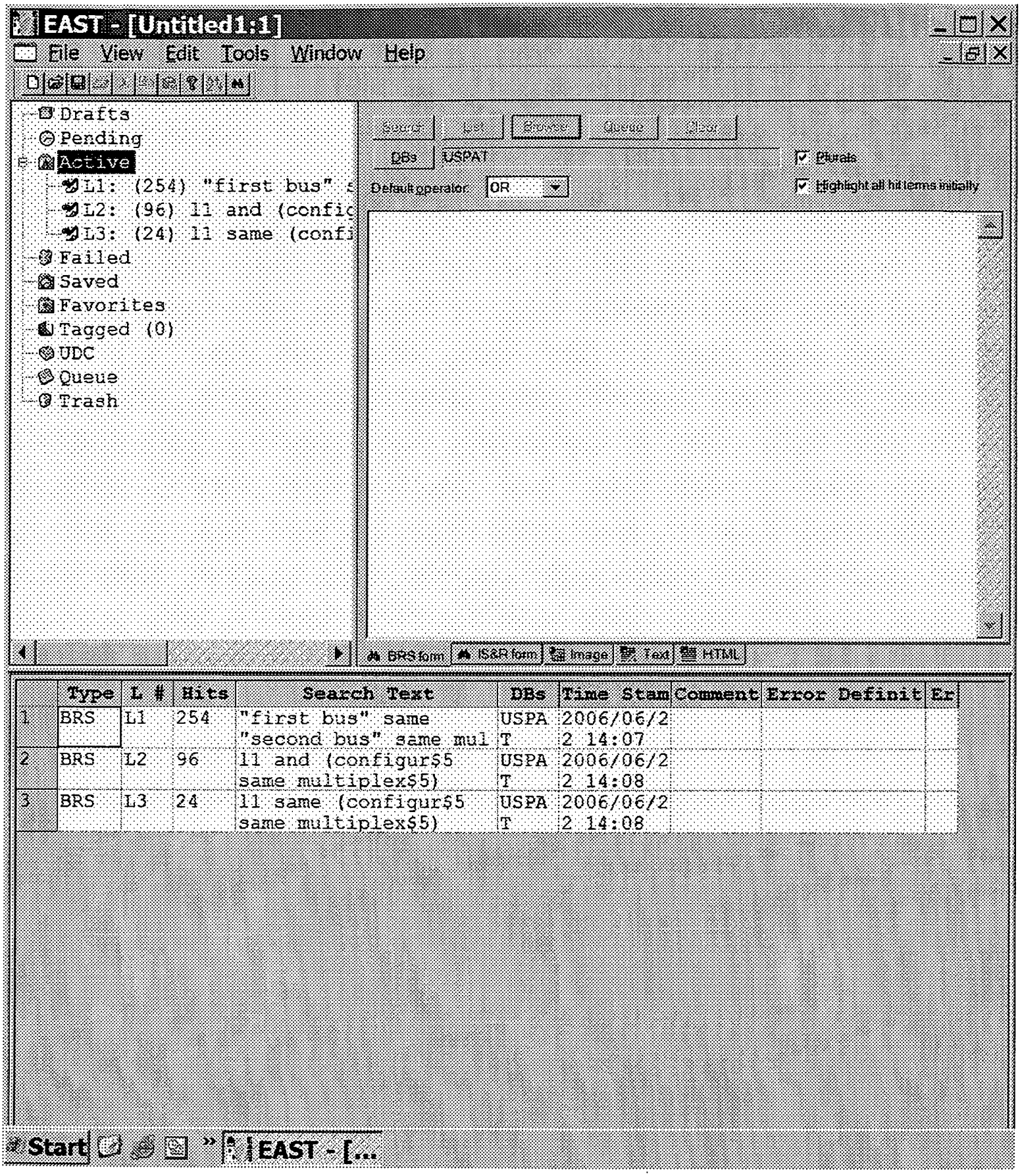
Recall Text | Clear | Interrupt

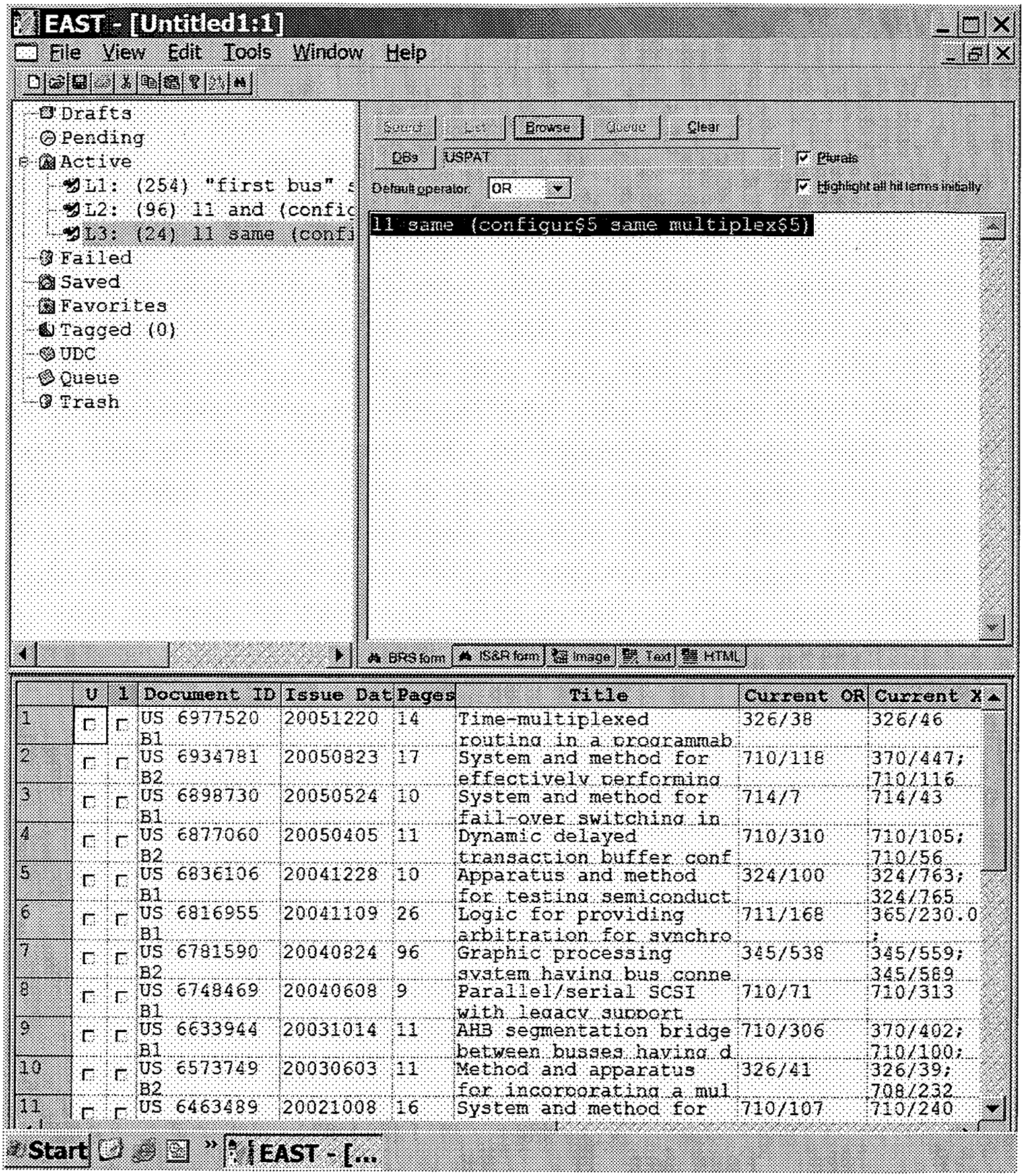
Search History

DATE: Thursday, June 22, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L5	L4 and (configur$5 same multiplex$3)	23	L5
L4	l1 and L3	59	L4
L3	710/316,302-304,104,72,305,107,307,317,37;713/1,323;370/464,362,364,357,916;712/29;709/253;716/12.ccls.	10927	L3
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L2	"first bus" same "second bus" same multiplex$3	46	L2
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
L1	"first bus" same "second bus" same multiplex$3	351	L1

END OF SEARCH HISTORY


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (254) "first bus" s
L2: (96) l1 and (confic
L3: (24) l1 same (confi
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
List
Browse
Queue
Clear
DBs
USPAT
Plurals
Default operator:
OR
Highlight all hit terms initially
BRS form
IS&R form
Image
Text
HTML
Type L # Hits Search Text DBs Time Stam Comment Error Definit Er
1 BRS L1 254 "first bus" same "second bus" same mul USPAT 2006/06/2 2 14:07
2 BRS L2 96 l1 and (configur$5 same multiplex$5) USPAT 2006/06/2 2 14:08
3 BRS L3 24 l1 same (configur$5 same multiplex$5) USPAT 2006/06/2 2 14:08
Start
EAST - [...


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (254) "first bus" s
L2: (96) l1 and (confic
L3: (24) l1 same (confi
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
Edit
Browse
Queue
Clear
DBs
USPAT
Plurals
Default operator:
OR
Highlight all hit terms initially
l1 same (configur$5 same multiplex$5)
BRS form
IS&R form
Image
Text
HTML
U
1
Document ID
Issue Dat
Pages
Title
Current OR
Current X
1 US B1 6977520 20051220 14 Time-multiplexed routing in a programmab 326/38 326/46
2 US B2 6934781 20050823 17 System and method for effectively performing 710/118 370/447; 710/116
3 US B1 6898730 20050524 10 System and method for fail-over switching in 714/7 714/43
4 US B2 6877060 20050405 11 Dynamic delayed transaction buffer conf 710/310 710/105; 710/56
5 US B1 6836106 20041228 10 Apparatus and method for testing semiconduct 324/100 324/763; 324/765
6 US B1 6816955 20041109 26 Logic for providing arbitration for synchro 711/168 365/230.0 ;
7 US B2 6781590 20040824 96 Graphic processing system having bus conne 345/538 345/559; 345/589
8 US B1 6748469 20040608 9 Parallel/serial SCSI with legacy support 710/71 710/313
9 US B1 6633944 20031014 11 AHB segmentation bridge between busses having d 710/306 370/402; 710/100;
10 US B2 6573749 20030603 11 Method and apparatus for incorporating a mul 326/41 326/39; 708/232
11 US 6463489 20021008 16 System and method for 710/107 710/240
Start
EAST - [...

Results for "(((first bus) and (second bus)<in>metadata) <and> (multiplex*<in>metadata))&..."

e-mail printer friendly

Your search matched **0** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

(((first bus) and (second bus)<in>metadata) <and> (multiplex*<in>metadata))<and

Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

No results were found.

Please edit your search criteria and try again. Refer to the Help pages if you need assistance revising your search.

Indexed by Inspec®

Results for "((first bus) and (second bus)<in>metadata)"

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Your search matched 1 of 1360403 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

New Search

Modify Search

((first bus) and (second bus)<in>metadata) Search

Check to search only within this results set

» Key

Display Format: Citation Citation & Abstract

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Hardware support: a cache lock mechanism without retry**
   Chuleui Hong; Kyeongmo Park; Yeong-Tae Song;
   Software Engineering, Artificial Intelligence, Networking and Parallel/Distributed Computing, 2005 and First ACIS International Workshop on Self-Assembling Wireless Networks, SNPD/SAWN 2005, Sixth International Conference on
   23-25 May 2005 Page(s):44 - 49
   Digital Object Identifier 10.1109/SNPD-SAWN.2005.41
   AbstractPlus | Full Text: PDF(128 KB) IEEE CNF
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Hardware support: a cache lock mechanism without retry

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Abstract
A lock mechanism is essential for synchronization on the multiprocessor systems. The conventional queuing lock has **two bus** traffics that are the initial and retry of the lock-read. This paper proposes the new locking protocol, called WPV (waiting processor variable) lock mechanism, which has only one lock-read bus traffic command. The WPV mechanism accesses the shared data in the initial lock-read phase that is held in the pipelined protocol until the shared data is transferred. The WPV mechanism also uses the cache state lock mechanism to reduce the locking overhead and guarantees the FIFO lock operations in the multiple lock contentions. In this paper, we also derive the analytical model of WPV lock mechanism as well as conventional memory and cache queuing lock mechanisms. The simulation results on the WPV lock mechanism show that about 50% of access time is reduced comparing with the conventional queuing lock mechanism.

Index Terms
Inspec
Controlled Indexing
cache storage multiprocessing systems protocols queueing theory synchronisation system buses

Non-controlled Indexing
FIFO lock operation bus traffics cache lock cache queuing hardware support lock-read locking protocol multiprocessor system pipelined protocol queuing lock synchronization waiting processor variable

Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.